REMARKS

The application has been reviewed in light of the Office Action dated November 10, 2004. Claims 1-14 were pending in this application., with claims 1 and 8 being in independent form. By this Amendment, new dependent claims 15-17 have been added, and claims 1 and 8-14 have been amended to place the claims in better form for reconsideration, without narrowing the scope of the claimed invention. Claims 1-17 are now pending in this application., with claims 1 and 8 being in independent form.

Claims 1-14 were objected to under 35 U.S.C. §132 as purportedly introducing new matter. Claims 1-14 were rejected under 35 U.S.C. §112, first paragraph, as purportedly failing to comply with the written description requirement.

By this Amendment, claims 1 and 8 have been amended to clarify the claimed invention. Verbatim support for the claim amendments may be found in the application at, for example, page 8, lines 10-12 (as noted in the Office Action).

Withdrawal of the objection under 35 U.S.C. §132 and the rejection under 35 U.S.C. §112, first paragraph is requested.

Claims 1-7 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,638,530 to Pawate in view of U.S. Patent No. 6,088,785 to Hudson. Claims 8-14 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Japanese Patent Application No. JP01264034A to Nakajima et al. in view of Pawate and further view of Hudson.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that the pending claims are patentable over the cited art, for at least the following reasons.

This application relates to a signal processing apparatus comprising an external memory

and a digital signal processor. The digital signal processor has an internal memory for storing a program to be executed. The internal program memory is typically limited in capacity. Therefore, digital signal processing programs are often stored for the digital signal processor in the external memory, and transferred to the internal memory, as necessary.

The signal processing apparatus of this application does not use a reset approach for program replacement (such as taught in Pawate) and can perform on-the-fly program replacement. More specifically, programs are expeditiously replaced by controlling a clock signal supplied to the internal memory of the digital signal processor during program replacement, without requiring initialization of the digital signal processor following program replacement. Each of independent claims 1 and 8 includes such features. Output of the clock signal to the digital signal processor is stopped to cause the digital signal processor to stop executing the program stored in the internal memory part. When output of the clock signal to the digital signal processor is stopped, the digital signal processor cannot access its internal memory. Output of the clock signal to the digital signal processor may be stopped in response to a request from the digital signal processor.

Pawate does not disclose or suggest such features.

Pawate, as understood by Applicant, is directed to a direct memory access scheme using a smart card as an interface between a host computer and assorted external devices (such as a fax, a modem, a microphone, a speaker). The smart card of Pawate has a DSP 170 onboard. A shared memory consisting of common memory 150 and attribute memory 160 can be accessed by the host computer as well as by the DSP. In addition, the DSP has its own memory which stores a program to be executed by the DSP. Paging by the DSP memory from the shared memory is performed only when the DSP is active and executing instructions (in smart mode), that is, while

the clock signal is actively supplied to the DSP.

It is contended in the Office Action that "Pawate teaches controlling the clock of the DSP to place the DSP into a power saving mode which allows the host computer to access the internal memory (internal to the DSP) (e.g. col. 13, line 59 to col. 14, line 48 and figure 2, elements 110-140, 180)."

Applicant respectfully disagrees. Pawate simply does not disclose or suggest controlling outputting of a clock signal to the digital signal processor so that programs stored in an external memory part can be forwarded to the internal memory part of the digital signal processor, as provided by the claimed invention set forth in independent claims 1 and 8.

Figure 2 of Pawate shows that elements 110-140 and 180 constitute smart card 100, but does not show or suggest that DSP 170 has an internal memory and therefore of course also fails to show or suggest how access to a DSP internal memory is controlled.

Pawate states as follows at col. 13, line 59 to col. 14, line 48:

> ... The host computer must load the reset and interrupt vectors of the DSP and the application program prior to switching the card into the smart mode. Since the host computer can access the entire memory on the card without consideration of the page sizes of the DSP (170), the memory pages not used by the DSP can be dedicated exclusively for use by the host computer.
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> An algorithm is executed in the following manner. If only a single algorithm is to be executed and loaded, **the host computer loads the desired algorithm to the memory of the DSP (170) and initializes the DSP (170). Next,** the host computer enables the AFEINT by setting the AINTEN bit allowing the host computer to be interrupted by the AFE card, for example, by the voice activated switch or the ring detect. **The host computer now may reduce power consumption of the system and turn off the clock of the DSP by setting the CLKON bit to zero.** The DSP (170) is placed into a hold mode and tri-stating the buses of the DSP, allowing the host computer to have quicker access to the remaining unused portion on the card (100). When the desired or expected external event occurs as indicated by the AFEINT, the host computer turns the clock of the DSP on and the DSP (170) begins executing the algorithm. Since the algorithm is already located into the memory

of the DSP (170), the computer does not delay in executing the algorithm since the algorithm is already loaded.

Further, multiple algorithms may be loaded and executed by DSP (170). The host computer initializes the DSP (170) and loads the operating system of the DSP. The operating system of the DSP loads various algorithms of the DSP into the various pages, for example, page one includes the first algorithm, and page two includes the second algorithm. The DSP (170) and host computer follows a pre-determined handshake protocol as set forth in the software examples. The commands and data may be exchanged easily between the host computer and the DSP (170) by using the communication registers as described hereinabove without halting the operation of the DSP. The operating system of the DSP controls the enabling the program/data of the DSP and the transmission of processed data by the DSP to the host computer. The following example is a list of the AFE interface connector-pin descriptions. See Example 10.

The software interface between the host computer and the DSP is as follows. As the smart card is powered up, the DSP is deactivated. Then the host computer is allowed to read/write the entire memory on the smart card. When the host computer switches the card from the standard mode to the smart mode, it performs the following functions. First, the host computer downloads the task to the shared memory. Note that the host computer will have to download the reset interrupt vectors starting at location zero. The host computer writes the signature pattern, for example, four times to the signature register. As the writing of signature pattern is seen four times by the control logic in the interface and controller circuit (180), the mode bit is set and the DSP is activated with start executing from the reset vector located in the shared memory. Example 11 illustrates a task control buffer used as handshake between application softwares in the host computer and the DSP.

Thus, it is abundantly clear as highlighted above that Pawate teaches that the host computer loads a desired program into the memory of the DSP and then initialize the DSP, and only after the program has been loaded into the DSP memory and the DSP has been initialized the host computer controls the clock of the DSP to place the DSP into a power-saving mode while the host computer accesses other functional portions of the smart card.

Applicant does not find teaching or suggestion in the cited art that supply of the clock signal to the digital signal processor is stopped to cause the digital signal processor to stop executing the program stored in the internal memory part, and when output of the clock signal to

the digital signal processor is stopped, the digital signal processor cannot access its internal memory.

Hudson, as understood by Applicant, is directed to an signal processing system which is adaptably reconfigurable for performing any of various signal processing functions. The Office Action cites Hudson as purportedly disclosing (a) control of output of a clock signal without initialization of the DSP, and (b) utilizing a lower frequency clock to place a subsystems into low power mode and halt mode which allows the subsystem to operate at a lower frequency.

However, Hudson, like Pawate, teaches that the clock signal is stopped for the purpose of conserving power consumption.

Although Hudson discloses swapping code into DSP memory from a DRAM, on an as-needed basis, Hudson does not disclose or suggest that the clock signal is stopped for the code swap operation. Indeed, Hudson clearly teaches that the DSP should continue to operate and run code from a first location of the DSP memory while the new code is being swapped into a second location of the DSP memory.

The Office Action cites Nakajima as purportedly showing use of a modem for modulating/demodulating communication data by using a signal processing apparatus which comprises a DSP. The Office Action acknowledges, however, that Nakajima does not disclose or suggest controlling outputting of the clock signal to the digital signal processor so that programs stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed invention.

In short, Applicant finds no teaching or suggestion in the cited art of controlling outputting of the clock signal to the digital signal processor so that programs stored in the external memory part can be forwarded to the internal memory part, as provided by the claimed

invention set forth in each of independent claims 1 and 8. Applicant simply does not find teaching or suggestion that supply of the clock signal to the digital signal processor is stopped to cause the digital signal processor to stop executing the program stored in the internal memory part, and when output of the clock signal to the digital signal processor is stopped, the digital signal processor cannot access its internal memory.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Allowance of this application is respectfully requested.

Respectfully submitted,

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